Assuming a 100 MHz clock (10 ns period), how many clock cycles are needed to implement a delay of at least 5 ms?

500000

How many bits are needed for a counter to implement a 5 ms delay with a 100 MHz clock?

19

Provide a summary of your synthesis warnings.

My synthesis only had errors when I was choosing the variables for my one shot detectors since I wasn’t completely sure which variables to use for each input. There weren’t any other warnings or critical errors. A different bug was that I didn’t implement all the inputs on the seven segment controller which caused errors in my waveform when simulating.

Indicate the number of Look-up Tables (LUT) and Input/Output (I/O) pins for your design.

LUT - 38

IO - 15

Summarize the results from your experiments comparing the debounced counter value to the non-debounced counter value.

For me, out of 100 button presses I could get anywhere from 3 to 20 bounces. This shows that the button itself is not very reliable and that a debouncer is always needed for accurate data when counting button presses.